What is claimed is:

1. A method comprising:

assigning a priority level to a cache allocation request;

identifying an allocation probability associated with the cache allocation request based on the priority level; and

identifying the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability.

2. A method as defined in claim 1, wherein assigning the priority level to the cache allocation request comprises assigning the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map.

3. A method as defined in claim 1, wherein assigning a priority level to the cache allocation request comprises assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application.

4. A method as defined in claim 1, wherein identifying the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability comprises comparing the allocation probability with at least one of a randomly-generated number and a predetermined number.

5. A method as defined in claim 1, wherein identifying the cache allocation request with one of an allocate condition and a bypass condition based on the allocation

probability comprises identifying the cache allocation request with the allocate condition in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.

6. A method as defined in claim 1, wherein identifying the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability comprises identifying the cache allocation request with the bypass condition in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number.

7. A method as defined in claim 1 further comprising allocating a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition and denying the cache allocation request in response to identifying the cache allocation request with the bypass condition.

8. A machine accessible medium storing instructions, which when executed, cause a processing system to:

assign a priority level to a cache allocation request;

identify an allocation probability associated with the cache allocation request based on the priority level; and

identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability.

9. A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to assign a priority level to the cache

allocation request by assigning the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map.

10. A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to assign the priority level to the cache allocation request by assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application.

11. A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to identify the cache allocation request with one of the allocate condition and the bypass condition by comparing the allocation probability with at least one of a randomly-generated number and a predetermined number.

12. A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to identify the cache allocation request with one of the allocate condition and the bypass condition based on the allocation probability by identifying the cache allocation request with the allocate condition in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.

13. A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to identify the cache allocation request

with one of the allocate condition and the bypass condition based on the allocation probability by identifying the cache allocation request with the bypass condition in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number.

14. A machine accessible medium as defined in claim 8, wherein the instructions, which when executed, cause the machine to allocate a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition, and to deny the cache allocation request in response to identifying the cache allocation request with the bypass condition.

15. A machine accessible medium as defined in claim 8, wherein the machine readable medium comprises one of a programmable gate array, application specific integrated circuit, erasable programmable read only memory, read only memory, random access memory, magnetic media, and optical media.

16. An apparatus comprising:

a cache to store one or more data blocks of cache allocation requests;

a priority assignment unit to assign a priority level to a cache allocation request; and

a cache controller to identify an allocation probability associated with the cache allocation request based on the priority level, and to identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability.

17. An apparatus as defined in claim 16, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application.

18. An apparatus as defined in claim 16, wherein the priority assignment unit comprises at least one of an operating system, a compiler, and an application specific integrated circuit.

19. An apparatus as defined in claim 16, wherein the cache controller is to assign the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map.

20. An apparatus as defined in claim 16, wherein the cache controller is to compare the allocation probability with at least one of a randomly-generated number and a predetermined number.

21. An apparatus as defined in claim 16, wherein the cache controller is to identify the cache allocation request with the allocate condition in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.

22. An apparatus as defined in claim 16, wherein the cache controller is to identify the cache allocation request with the bypass condition in response to the

allocation probability being less than at least one of randomly-generated number and a pre-determined number.

23. An apparatus as defined in claim 16, wherein the cache controller is to allocate a portion of the cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition.

24. A processor system comprising:

a static random access memory (SRAM) to store one or more data blocks of cache allocation requests; and

a processor coupled to the SRAM, the processor to:

assign a priority level to a cache allocation request;

identify an allocation probability associated with the cache allocation request based on the priority level; and

identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability.

25. A processor system as defined in claim 24, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application.

26. A processor system as defined in claim 24, wherein the processor is to assign the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map.

27. A processor system as defined in claim 24, wherein the processor is to compare the allocation probability with at least one of a randomly-generated number and a predetermined number.

28. A processor system as defined in claim 24, wherein the processor is to identify the cache allocation request with the allocate condition in response to in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.

29. A processor system as defined in claim 24, wherein the processor is to identify the cache allocation request with the bypass condition in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number.

30. A processor system as defined in claim 24, wherein the processor is to allocate a portion of the SRAM to the cache allocation request in response to identifying the cache allocation request with the allocate condition.